Introduction to LVDS

Chapter 1

1.0.0 INTRODUCTION TO LVDS

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces or a balanced cable.

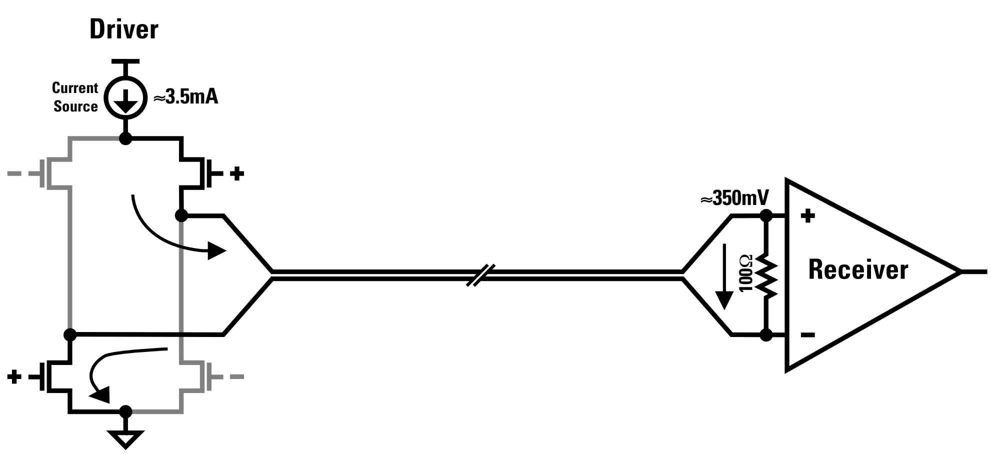
1.1.0 THE TREND TO LVDS

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics and photo-realistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high-speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from board-to-board or box-to-box, however, requires an extremely high-performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise and is inexpensive. Unfortunately existing solutions are a compromise of these four basic ingredients: **performance, power, noise, and cost.**

1.2.0 GETTING SPEED WITH LOW NOISE AND LOW POWER

LVDS is a low swing, differential signaling technology which allows single channel data transmission at hundreds or even thousands of Megabits per second (Mbps). Its low swing and current-mode driver outputs create low noise and provide very low power consumption across frequency.

1.2.1 How LVDS Works



Simplified Diagram of LVDS Driver and Receiver Connected via 100Ω Differential Impedance Media

National's LVDS outputs consist of a current source (nominal 3.5mA) which drives the differential pair line. The basic receiver has high DC input impedance, so the majority of driver current flows across the 100Ω termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 Why Low Swing Differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers which looks at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. And, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low — almost flat — power consumption across frequency is obtained. Switching spikes in the driver are very small, so that I_{CC} does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5mA x 350mV = 1.2mW) is very small in magnitude.

1.2.3 The LVDS Standard

LVDS is currently standardized by two different standards:

TIA/EIA (Telecommunications Industry Association/Electronic Industries Association)
- ANSI/TIA/EIA-644 (LVDS) Standard

IEEE (Institute for Electrical and Electronics Engineering)
- IEEE 1596.3

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644 (LVDS) Standard
Note: Actual datasheet specifications may be significantly better.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change to V_{OD}|		50	|mV|
ΔV_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short Circuit Current		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)	0.26	30% of t_{ui}†	ns
I_{IN}	Input Current		20	|μA|
V_{TH}	|Threshold Voltage|		±100	mV
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e. bit width).

The ANSI/TIA/EIA standard notes a recommend a maximum data rate of 655Mbps (based on one set of assumptions) and it also provides a theoretical maximum of 1.923Gbps based on a loss-less medium. This allows the referencing standard to specify the maximum data rate required depending upon required signal quality and media length/type. The standard also covers minimum media specifications, failsafe operation of the receiver under fault conditions, and other configuration issues such as multiple

receiver operation. The ANSI/TIA/EIA-644 standard was approved in November 1995. National Semiconductor held the editor position for this standard and chairs the sub committee responsible for electrical TIA interface standards. Currently the 644 spec is being revised to include additional information about multiple receiver operation. The revised (to be known as TIA-644-A) is expected to be balloted upon in calendar year 2000.

The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the IEEE 1596.3 standard. The SCI-LVDS standard also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB traces or cable, thereby serving a broad range of applications in many industry segments.

1.2.4 A Quick Comparison between Differential Signaling Technologies

Parameter	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2 to ±5 V	±600-1000mV	±250-450mV
Receiver Input Threshold	±200mV	±200-300mV	±100mV
Data Rate	<30Mbps	>400Mbps	>400Mbps

Parameter	RS-422	PECL	LVDS*
Supply Current Quad Driver (no load, static)	60mA (max)	32-65mA (max)	8.0mA
Supply Current Quad Receiver (no load, static)	23mA (max)	40mA (max)	15mA (max)
Propagation Delay of Driver	11ns (max)	4.5ns (max)	1.7ns (max)
Propagation Delay of Receiver	30ns (max)	7.0ns (max)	2.7ns (max)
Pulse Skew (Driver or Receiver)	N/A	500ps (max)	400ps (max)

*LVDS devices noted are DS90LV047A/048A

The chart above compares basic LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are one-tenth of RS-422 and also traditional TTL/CMOS levels. Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

1.2.5 Easy Termination

Whether the LVDS transmission medium consists of a cable or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed (edge rates) signals. If the medium is not properly terminated, signals reflect from the end of the cable or trace and may interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions and provides the optimum signal quality.

To prevent reflections, LVDS requires a terminating resistor that is matched to the actual cable or PCB traces differential impedance. Commonly 100Ω media and terminations are employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input.

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL can require more complex termination than the one-resistor solution for LVDS. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ω resistor across the receiver input.

1.2.6 Maximum Switching Speed

Maximum switching speed of a LVDS Interface is a complex question, and its answer depends upon several factors. These factors are the performance of the Line Driver (Edge Rate) and Receiver, the bandwidth of the media, and the required signal quality for the application.

Since the driver outputs are very fast, the limitation on speed is commonly restricted by:

1. How fast TTL data can be delivered to the driver – in the case of simple PHY devices that translate a TTL/CMOS signal to LVDS (i.e. DS90LV047A)

2. Bandwidth performance of the selected media (cable) – type and length dependent

In the case of LVDS drivers, like the DS90LV047A, its speed is limited by how fast the TTL data can be delivered to the driver.

National's Channel Link devices capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream — more about this later.

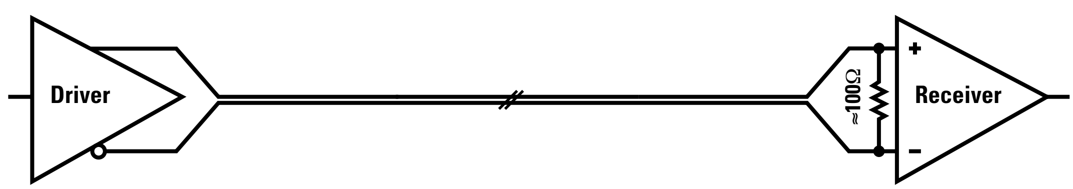
1.2.7 Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination, for 90mW power consumption — 75 times more than LVDS.

LVDS devices are implemented in CMOS processes, which provide low static power consumption. The circuit design of the drivers and receiver require roughly one-tenth the power supply current of PECL/ECL devices (quad device comparison).

Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power through its current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. Frequency plot for LVDS is virtually flat between 10MHz and 100MHz for the quad devices (DS90C031/2), <50mA total for driver and receiver at 100MHz. Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

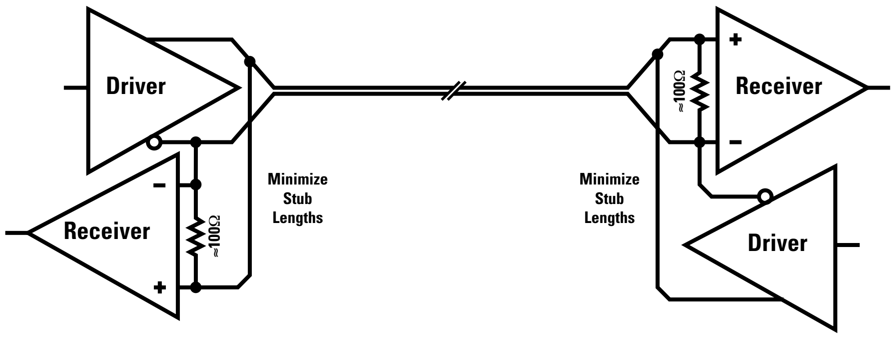
1.2.8 LVDS Configurations



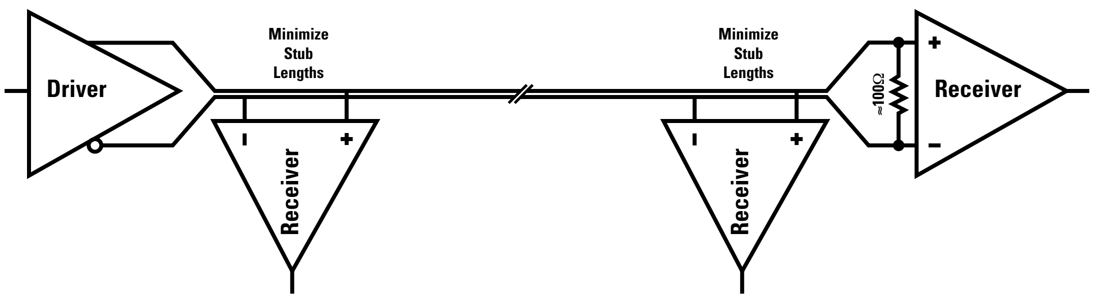
Point-to-Point Configuration

LVDS drivers and receivers are commonly used in a point-to-point configurations as shown above. However, other topologies/configurations are also possible.

The configuration shown next allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (<10m). (See also Bus LVDS Devices (Chapter 6) - which are designed for double termination loads and provide full LVDS compatible levels).



Bi-Directional Half-Duplex Configuration



Multidrop Configuration

A multidrop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than12mm – application dependent). (See also Bus LVDS Devices, which are designed for double termination loads and provide LVDS compatible levels)

Dedicated point-to-point links provide the best signal quality due to the clear path they provide. LVDS has many advantages that make it likely to become the next famous data transmission standard for data rates from DC to hundreds of Mbps and short haul distances in the tens of meters. In this role, LVDS will far exceed the 20Kbps to 30Mbps rates of the common RS-232, RS-422, and RS-485 standards.

1.3.0 AN ECONOMICAL INTERFACE - SAVE MONEY TOO

LVDS can save money in several important ways:

1. National's LVDS solutions are inexpensive CMOS implementations as compared to custom solutions on elaborate processes.

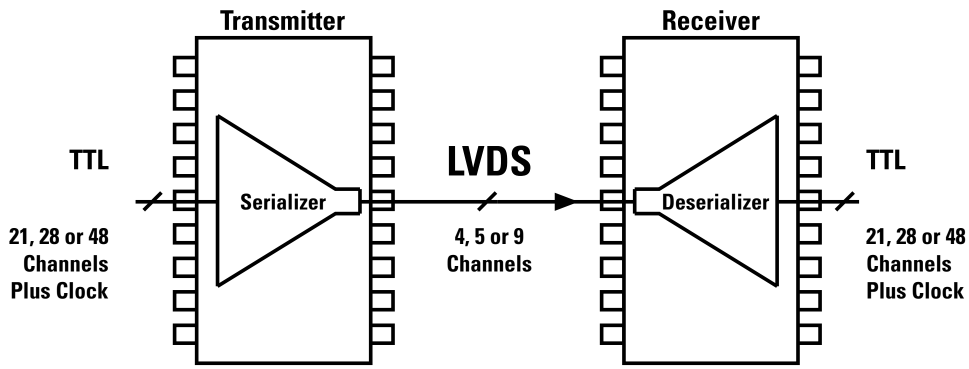
2. High performance can be achieved using low cost, off-the-shelf CAT3 cable and connectors, and/or FR4 material.

3. LVDS consumes very little power, so power supplies, fans, etc. can be reduced or eliminated.

4. LVDS is a low noise producing, noise tolerant technology – power supply and EMI noise headaches are greatly minimized.

5 LVDS transceivers are relatively inexpensive and can also be integrated around digital cores providing a higher level of integration.

6. Since LVDS can move data so much faster than TTL, multiple TTL signals can be serialized or mux'ed into a single LVDS channel, reducing board, connector, and cable costs.



National's Channel Link Chipsets Convert a TTL Bus into a Compact LVDS Data Stream and Back to TTL.

In fact, in some applications, the PCB, cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic (user-friendly) system.

1.4.0 LVDS APPLICATIONS

The high-speed and low power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	(Box-to-box & rack-to-rack)	
Multimedia peripheral links		

1.5.0 NATIONAL'S WIDE RANGE OF LVDS SOLUTIONS

National Semiconductor offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV047A/DS90LV048A quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains singles, duals and quad footprints.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI) devices. These parts provide a high bandwidth, low power, small size, low power interface enabling XGA/SXGA/UXGA and beyond displays for notebook and monitor applications.

Another more generalized use of LVDS is in the National Channel Link family, which can take 21, 28 or 48-bits of TTL data and converts it to 3, 4 or 8 channels of LVDS data plus LVDS clock. These devices provide fast data pipes (up to 5.4 Gbps throughput) and are well suited for high-speed network hubs or routers applications or anywhere a low cost, high-speed link is needed. Their serializing nature provides an overall savings to system cost as cable and connector physical size and cost are greatly reduced.

Bus LVDS is an extension of the LVDS Line drivers and receivers family. They are specifically designed for multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30 to 50Ω range. Bus LVDS drivers provide about 10mA of output current so that they provide

LVDS swings with heavier termination loads. Transceivers and Repeaters are currently available in this product family. A 10-bit Serializer and Deserializer family of devices is available that embeds and recovers clock from a single serial stream. This chip set also provides a high level of integration with on-chip clock recovery circuitry. Certain Deserializers provide a random data lock capability (An Industry First). The Deserializer can be hot-plugged into a live data bus and does not require PLL training.

Special Functions are also being developed using LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs is available (DS92CK16) and also a line of crosspoint switches is being introduced.

Over 75 different LVDS products are currently offered by National. For the latest in product information, and news, please visit National's LVDS web site at: **www.national.com/appinfo/lvds/**

1.6.0 CONCLUSION

National's LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.

NOTES